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	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef
1	☐	☐	US 6700143 B2	20040302	16	Dummy structures that protect circuit elements during polishing	257/288	257/296; 257/750;
2	☑	☐	US 6699776 B2	20040302	10	MOSFET gate insulating film and method of manufacturing the same	438/585	438/197; 438/199;
3	☑	☐	US 6696333 B1	20040224	19	Method of making integrated circuit with MOSFETs having bi-layer metal	438/230	438/275; 438/303;
4	☑	☐	US 6660664 B1	20031209	15	Structure and method for formation of a blocked silicide resistor	438/791	438/257; 438/260;
5	☑	☐	US 6657267 B1	20031202	8	Semiconductor device and fabrication technique using a high-K li	257/410	257/213; 257/288;
6	☑	☐	US 6643186 B2	20031104	65	Nonvolatile memory structures and fabrication methods	365/185.33	257/E21.625; 257/E21.689;
7	☑	☐	US 6617636 B2	20030909	63	Nonvolatile memory structures and fabrication methods	257/315	257/E21.625; 257/E21.689;
8	☑	☐	US 6617212 B2	20030909	14	Semiconductor device and method for fabricating the same using damasc	438/270	257/288; 257/330;
9	☑	☐	US 6602721 B2	20030805	19	Method for fabricating ferroelectric memory device and method for fabric	438/3	438/240
10	☑	☐	US 6583012 B1	20030624	15	Semiconductor devices utilizing differently composed metal-based in-l	438/275	257/E21.637; 438/197;
11	☑	☐	US 6559055 B2	20030506	16	Dummy structures that protect circuit elements during polishing	438/692	257/E21.625; 257/E21.680;

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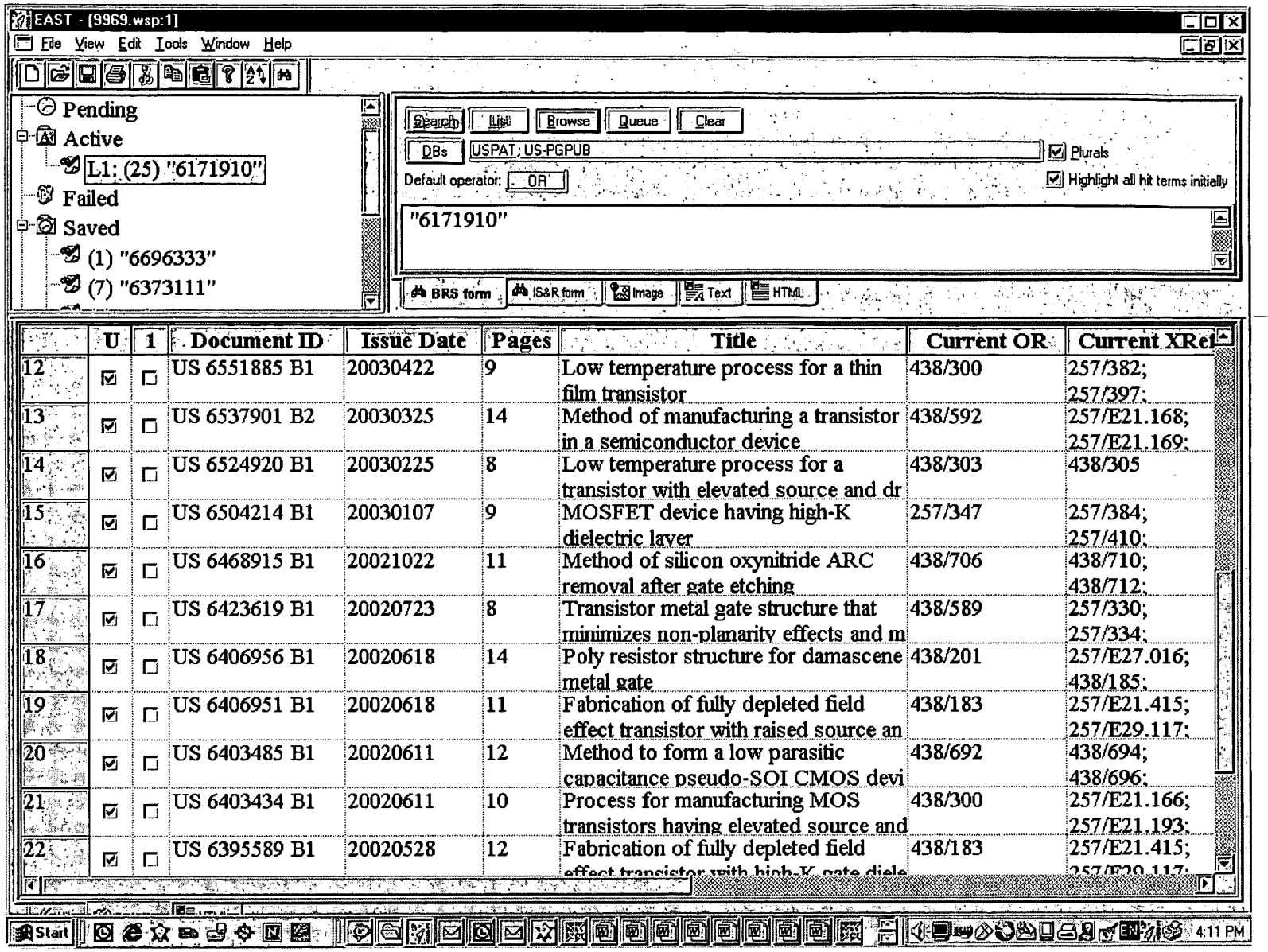
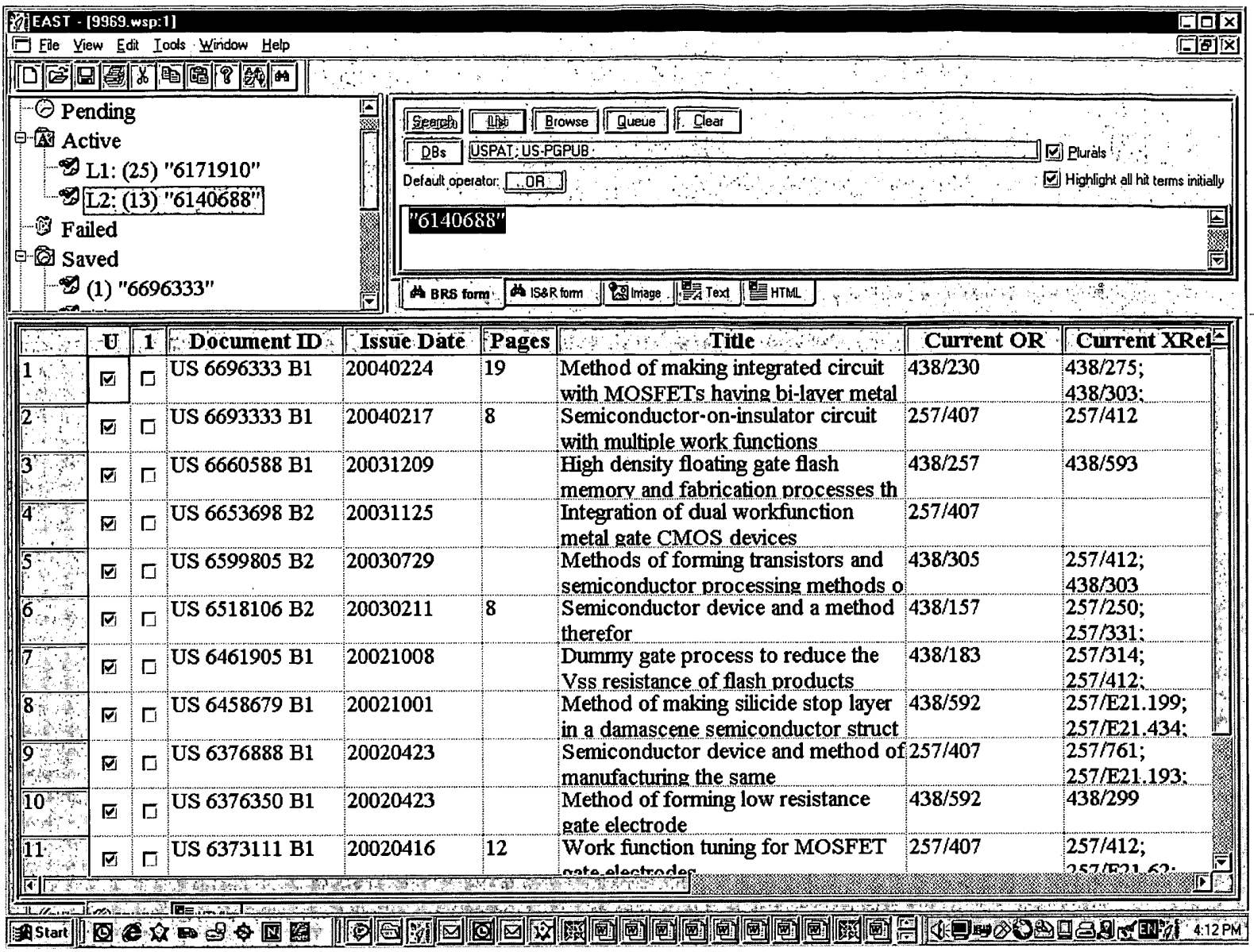
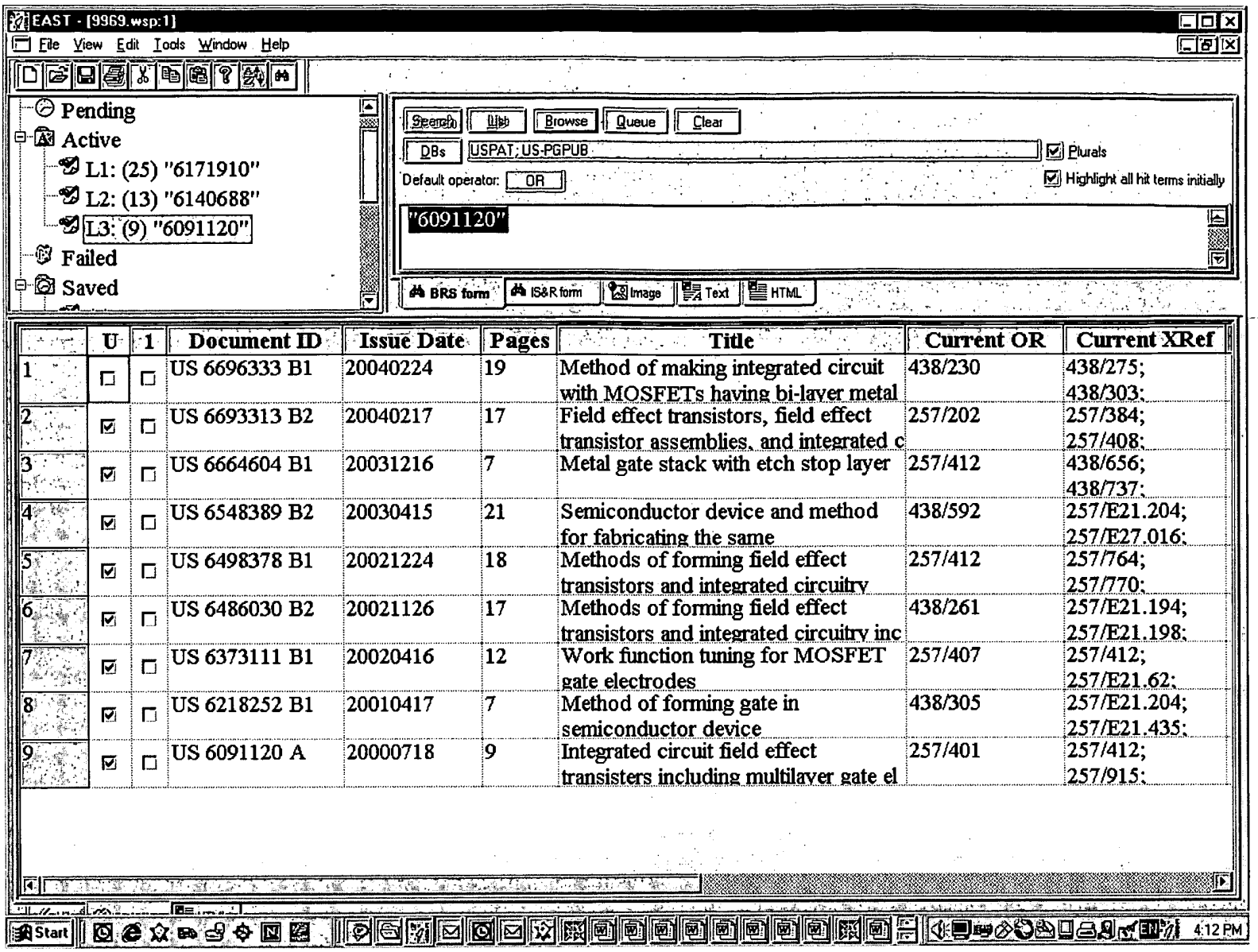


	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef
12	☑	☐	US 6551885 B1	20030422	9	Low temperature process for a thin film transistor	438/300	257/382; 257/397;
13	☑	☐	US 6537901 B2	20030325	14	Method of manufacturing a transistor in a semiconductor device	438/592	257/E21.168; 257/E21.169;
14	☑	☐	US 6524920 B1	20030225	8	Low temperature process for a transistor with elevated source and dr	438/303	438/305
15	☑	☐	US 6504214 B1	20030107	9	MOSFET device having high-K dielectric layer	257/347	257/384; 257/410;
16	☑	☐	US 6468915 B1	20021022	11	Method of silicon oxynitride ARC removal after gate etching	438/706	438/710; 438/712;
17	☑	☐	US 6423619 B1	20020723	8	Transistor metal gate structure that minimizes non-planarity effects and m	438/589	257/330; 257/334;
18	☑	☐	US 6406956 B1	20020618	14	Poly resistor structure for damascene metal gate	438/201	257/E27.016; 438/185;
19	☑	☐	US 6406951 B1	20020618	11	Fabrication of fully depleted field effect transistor with raised source an	438/183	257/E21.415; 257/E29.117;
20	☑	☐	US 6403485 B1	20020611	12	Method to form a low parasitic capacitance pseudo-SOI CMOS devi	438/692	438/694; 438/696;
21	☑	☐	US 6403434 B1	20020611	10	Process for manufacturing MOS transistors having elevated source and	438/300	257/E21.166; 257/E21.193;
22	☑	☐	US 6395589 B1	20020528	12	Fabrication of fully depleted field effect transistor with high-K gate diele	438/183	257/E21.415; 257/E29.117;



	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef
1	☑	☐	US 6696333 B1	20040224	19	Method of making integrated circuit with MOSFETs having bi-layer metal	438/230	438/275; 438/303;
2	☑	☐	US 6693333 B1	20040217	8	Semiconductor-on-insulator circuit with multiple work functions	257/407	257/412
3	☑	☐	US 6660588 B1	20031209		High density floating gate flash memory and fabrication processes th	438/257	438/593
4	☑	☐	US 6653698 B2	20031125		Integration of dual workfunction metal gate CMOS devices	257/407	
5	☑	☐	US 6599805 B2	20030729		Methods of forming transistors and semiconductor processing methods o	438/305	257/412; 438/303
6	☑	☐	US 6518106 B2	20030211	8	Semiconductor device and a method therefor	438/157	257/250; 257/331;
7	☑	☐	US 6461905 B1	20021008		Dummy gate process to reduce the Vss resistance of flash products	438/183	257/314; 257/412;
8	☑	☐	US 6458679 B1	20021001		Method of making silicide stop layer in a damascene semiconductor struct	438/592	257/E21.199; 257/E21.434;
9	☑	☐	US 6376888 B1	20020423		Semiconductor device and method of manufacturing the same	257/407	257/761; 257/E21.193;
10	☑	☐	US 6376350 B1	20020423		Method of forming low resistance gate electrode	438/592	438/299
11	☑	☐	US 6373111 B1	20020416	12	Work function tuning for MOSFET gate electrodes	257/407	257/412;



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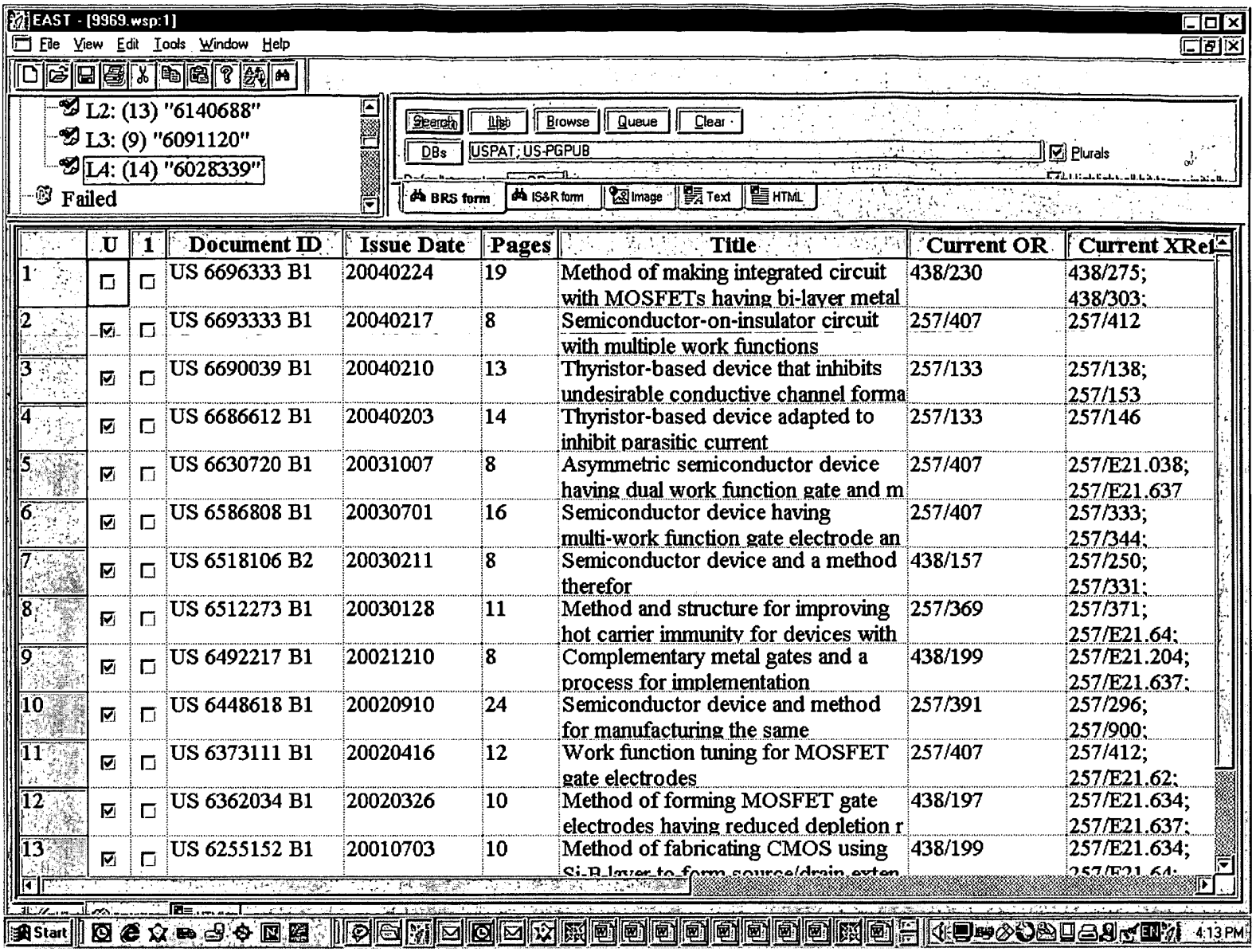
1	☐	☐	US 6696333 B1	20040224	19	Method of making integrated circuit with MOSFETs having bi-layer metal	438/230	438/275; 438/303;
2	☑	☐	US 6693313 B2	20040217	17	Field effect transistors, field effect transistor assemblies, and integrated c	257/202	257/384; 257/408;
3	☑	☐	US 6664604 B1	20031216	7	Metal gate stack with etch stop layer	257/412	438/656; 438/737;
4	☑	☐	US 6548389 B2	20030415	21	Semiconductor device and method for fabricating the same	438/592	257/E21.204; 257/E27.016;
5	☑	☐	US 6498378 B1	20021224	18	Methods of forming field effect transistors and integrated circuitry	257/412	257/764; 257/770;
6	☑	☐	US 6486030 B2	20021126	17	Methods of forming field effect transistors and integrated circuitry inc	438/261	257/E21.194; 257/E21.198;
7	☑	☐	US 6373111 B1	20020416	12	Work function tuning for MOSFET gate electrodes	257/407	257/412; 257/E21.62;
8	☑	☐	US 6218252 B1	20010417	7	Method of forming gate in semiconductor device	438/305	257/E21.204; 257/E21.435;
9	☑	☐	US 6091120 A	20000718	9	Integrated circuit field effect transisters including multilayer gate el	257/401	257/412; 257/915;



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1	☐	☐	US 6696333 B1	20040224	19	Method of making integrated circuit with MOSFETs having bi-layer metal	438/230	438/275; 438/303;
2	☑	☐	US 6693333 B1	20040217	8	Semiconductor-on-insulator circuit with multiple work functions	257/407	257/412
3	☑	☐	US 6690039 B1	20040210	13	Thyristor-based device that inhibits undesirable conductive channel forma	257/133	257/138; 257/153
4	☑	☐	US 6686612 B1	20040203	14	Thyristor-based device adapted to inhibit parasitic current	257/133	257/146
5	☑	☐	US 6630720 B1	20031007	8	Asymmetric semiconductor device having dual work function gate and m	257/407	257/E21.038; 257/E21.637
6	☑	☐	US 6586808 B1	20030701	16	Semiconductor device having multi-work function gate electrode an	257/407	257/333; 257/344;
7	☑	☐	US 6518106 B2	20030211	8	Semiconductor device and a method therefor	438/157	257/250; 257/331;
8	☑	☐	US 6512273 B1	20030128	11	Method and structure for improving hot carrier immunity for devices with	257/369	257/371; 257/E21.64;
9	☑	☐	US 6492217 B1	20021210	8	Complementary metal gates and a process for implementation	438/199	257/E21.204; 257/E21.637;
10	☑	☐	US 6448618 B1	20020910	24	Semiconductor device and method for manufacturing the same	257/391	257/296; 257/900;
11	☑	☐	US 6373111 B1	20020416	12	Work function tuning for MOSFET gate electrodes	257/407	257/412; 257/E21.62;
12	☑	☐	US 6362034 B1	20020326	10	Method of forming MOSFET gate electrodes having reduced depletion r	438/197	257/E21.634; 257/E21.637;
13	☑	☐	US 6255152 B1	20010703	10	Method of fabricating CMOS using Si-B layer to form source/drain exten	438/199	257/E21.634; 257/E21.64;

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1	☐	☐	US 20030151074 A1	20030814	12	Work function tuning for mosfet gate electrodes	257/200	257/E21.62; 257/E21.623;
2	☐	☐	US 6696333 B1	20040224	19	Method of making integrated circuit with MOSFETs having bi-layer metal	438/230	438/275; 438/303;
3	☑	☐	US 6693333 B1	20040217	8	Semiconductor-on-insulator circuit with multiple work functions	257/407	257/412
4	☑	☐	US 6617624 B2	20030909	12	Metal gate electrode stack with a passivating metal nitride layer	257/288	257/408; 257/413;
5	☑	☐	US 6518106 B2	20030211	8	Semiconductor device and a method therefor	438/157	257/250; 257/331;
6	☐	☐	US 6506676 B2	20030114	6	Method of manufacturing	438/683	257/E21.17; 438/580;
7	☐	☐	US 6373111 B1	20020416	12	Work function tuning for MOSFET gate electrodes	257/407	257/412; 257/E21.62;

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